The following listing of claims will replace all prior versions of claims in the application.

Claim 1. (presently amended) A method for depositing multiple metal layers on a semiconductor substrate, comprising:

contacting a semiconductor substrate with an electrolytic plating composition, the plating composition comprising a copper metal source and a second metal source distinct from copper;

electrolytically depositing a first metal layer of copper~~, from the copper metal source,~~ on the semiconductor substrate at a first reduction potential;

electrolytically depositing a second metal layer~~, from the second metal source,~~ on the semiconductor substrate at a second reduction potential distinct from the first reduction potential.

Claim 2. (original) The method of claim 1 wherein the first metal layer is a substantially homogenous copper metal layer.

Claim 3. (original) The method of claim 1 wherein the second metal layer is a copper alloy.

Claim 4. (original) The method of claim 1 wherein the second metal layer comprises one or more of zinc, tantalum, beryllium, magnesium, nickel, titanium, tin, palladium, silver and cadmium.

Claim 5. (original) The method of claim 1 wherein the second metal layer is a copper alloy that comprises one or more of zinc, tantalum, beryllium, magnesium, nickel, titanium, tin, palladium, silver and cadmium.

Claim 6. (original) The method of claim 1 wherein the first and second reduction potentials differ by at least about 0.2 V.

Claim 7. (original) The method of claim 1 wherein a plurality of first metal layer are deposited with a plurality of alternating second metal layers.

Claim 8. (presently amended) The method of claim 1 wherein the first metal layer is effectively conductive and the second metal layer is substantially less conductive than the first metal layer.

Claim 9. (original) The method of claim 1 wherein the first metal layer functions as an electrical circuit, and the second metal layer functions as an insulator layer.

Claim 10. (original) The method of claim 1 wherein the substrate is a lead of a semiconductor device, or an interconnect of a semiconductor device.

Claims 11-20. (cancelled)

Claim 21. A method for depositing multiple metal layers on an electronic device substrate ~~chosen from a semiconductor substrate, a semiconductor package substrate, a multi-chip module, chip capicator, chip resistor, lead frame, or an opto-electronic device~~, comprising:

contacting the electronic device substrate with an electrolytic plating composition, the plating composition comprising a first metal source and a second metal source distinct from the first metal;

electrolytically depositing a layer of the first metal ~~layer, from the second metal source,~~ on the substrate at a first reduction potential;

electrolytically depositing a second metal layer on the substrate, from the second metal source, at a second reduction potential distinct from the first reduction potential.

Claim 22. (original) The method of claim 21 wherein the substrate is a semiconductor substrate.

Claim 23. (original) The method of claim 21 wherein the substrate is a semiconductor package substrate.

Claim 24. (original) The method of claim 21 wherein the substrate is a multi-chip module, chip capicator, chip resistor, lead frame, or an opto-electronic device.

Claim 25. (original) The method of claim 21 wherein the first metal layer is a substantially homogenous tin metal layer.

Claim 26. (original) The method of claim 21 wherein the second metal layer is a tin alloy.

Claim 27. (original) The method of claim 21 wherein the second metal layer comprises one or more of zinc, nickel, silver, antimony, bismuth, indium, cobalt, and copper.

Claim 28. (original) The method of claim 21 wherein the first and second reduction potentials differ by at least about 0.2 V.

Claim 29. (original) The method of claim 21 wherein a plurality of first metal layer are deposited with a plurality of alternating second metal layers.

Claim 30. (presently amended) The method of ~~claim 21~~ ~~any one of claims 21 through 30~~ wherein the first metal layer is effectively conductive and the second metal layer is substantially less conductive than the first metal layer.

Claim 31. (original) The method of claim 21 wherein the first and second metal layers are deposited from a single plating bath.